MHTL

INTEGRATED CIRCUITS

MC660 SERIES

MHTL

INTEGRATED CIRCUITS

INDEX

NUMERICAL INDEX
(Functions and Characteristics)

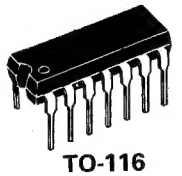
V_{CC} = 15 V ±1.0 V, T_A = 25°C, Case 93

Function	Type -30 to +75°C	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg	Page No.
Expandable Dual 4-Input NAND Gate (active pullup)	MC660P	10	110	88/26 ①	3-8
Expandable Dual 4-Input NAND Gate (passive pullup)	MC661P	10	125	88/26 ①	3-10
Expandable Dual 4-Input Line Driver	MC662P	30	140	180/26 ①	3-20
Dual J-K Flip-Flop	MC663P	9	–	200	3-22
Master-Slave R-S Flip-Flop	MC664P	8	–	160	3-24
Quad 2-Input NAND Gate (passive pullup)	MC668P	10	125	176/52 ①	3-16
Dual 4-Input Expander	MC669P	–	–	–	3-26
Triple 3-Input NAND Gate (passive pullup)	MC670P	10	125	132/39 ①	3-12
Triple 3-Input NAND Gate (active pullup)	MC671P	10	110	132/39 ①	3-14
Quad 2-Input NAND Gate (active pullup)	MC672P	10	110	176/52 ①	3-18

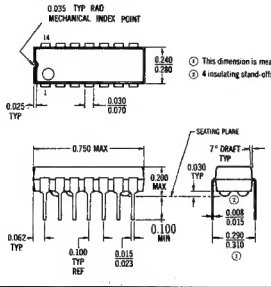
① Input High/Inputs Low

UNIBLOC* PLASTIC PACKAGE CASE 93

*Trademark of Motorola Inc.



TO-116



MAXIMUM RATINGS $T_A = 25^oC$

Rating	Symbol	Value	Unit
Power Supply Voltage Continuous Pulsed, < 1.0 s	V_{CC}	 18 20	Vdc
Input Voltage (MC669P Expanders Reverse Voltage)	V_{in}	−1.0/+18 18	Vdc
Output Current (into outputs) MC660, 661, 670, 671, 668, 672 MC662 MC663 MC664 MC669	—	 30 60 28 26 —	mAdc
Input Reverse Current @ 20 V	I_R	0.5	mAdc
Forward Current (individual) MC669P	I_F	30	mAdc
Operating Temperature Range	T_A	−30 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

TEST LIMITS TOLERANCE

$T_A = \pm 3^oC$ $V_R = \pm 1\%$ $V_{CC} = \pm 1\%$ $V_{IL} = \pm 1\%$ $V_{IH} = \pm 1\%$ $V_F = \pm 1\%$ $I_{OL} = \pm 1\%$ $I_{OH} = \pm 1\%$

DEFINITIONS

CP Clock Pulse

I_{CEX} Collector-to-emitter leakage of the output transistor

I_{CCH} V_{CC} current drain when all inputs are high

I_{CCL} V_{CC} current drain when all inputs are low

I_F Forward current of input diodes for unit input load

$2\,I_F$ Forward current of input diodes which are equal to twice unit load

I_{OH} Test current flowing into the output pin when output is high. (Negative)

I_{OL} Test current flowing into output pin when output is low

I_R Reverse current of input diodes with V_R applied

$2\,I_R$ Reverse current of two input diodes with V_R applied

I_{SC} Short-circuit current obtained from device output when output is high

t_{pd+} Propagation delay time for a positive-going output pulse

t_{pd-} Propagation delay time for a negative-going output pulse

V_{CC} Device power supply voltage

V_{CCH} High power supply voltage

V_{CCL} Low power supply voltage

V_{CEX} Collector-to-emitter voltage of the output transistor

V_F Input voltage when measuring I_F

V_{IH} Threshold voltage for high input voltage state

V_{IL} Threshold voltage for low input voltage state

V_{OH} Output high voltage state with I_{OH} flowing out of pin

V_{OL} Output low voltage state with I_{OL} flowing into pin

V_R Reverse voltage for input diode leakage test

V_X Threshold voltage for low input voltage state on expander unit

GENERAL RULES

- The number of load circuits that may be driven from an output is determined by the input loading factor. The summation of input loading should not exceed the drive capability of the output.
- The outputs of the passive pullup gates may be tied together to perform the wired-collector OR function. For each added gate subtract 1.2 output loading factor (fan-out).
- The outputs of the active pullup devices should not be tied together.

HIGH THRESHOLD LOGIC

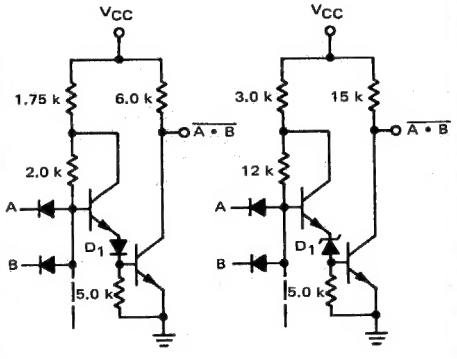
The High Threshold Logic (MHTL) family of integrated circuit devices was developed for applications requiring a higher degree of inherent electrical noise immunity than is available with the more standard forms of integrated circuit logic families. The basic MHTL logic gate is similar to the Diode Transistor Logic (MDTL) gate circuit as can be seen in Figure 1. A considerably larger input threshold characteristic is exhibited by the MHTL devices by using a reversed biased base-emitter junction which operates in the breakdown avalanche mode (sometimes referred to as zener operation) as compared to a forward biased diode junction for the corresponding D_1 element in the MDTL gate. A typical 7.5 volt input signal is required to turn on the MHTL output inverting transistor while a 1.5 volt signal is necessary for MDTL.

The higher threshold characteristic of MHTL requires a higher V_{CC} supply and is specified at 15 volts ±1.0 V tolerance. In order to keep the power dissipation within reasonable levels, higher values of resistance are used in MHTL than for corresponding resistors in the MDTL circuit. These resistance values also allow the outputs of gates to be interconnected to provide the "wired - or" logic function. The propagation delay of MHTL is in the order of 110 nanoseconds and consequently is a relatively slow logic family, a property which aids in rejecting noise. A comparison of transfer curves is made in Figure 2 illustrating the large logic swing available from MHTL.

An active output pullup configuration is available for the MHTL devices and is shown in Figure 3. The active output arrangement will allow the circuits to handle capacitive loads at a higher speed than is obtainable with the passive pullup configuration. Additionally, the impedance in the high state is considerably less, and consequently makes the family more immune to electrical noise. The active output configuration also allows for a more powerful arrangement to interface with discrete components.

In summary the MHTL devices may be characterized as an integrated circuit family with a high degree of inherent noise immunity, a high input threshold and a large logic swing. These characteristics make the line very attractive for use where electrical noise is an important consideration, as well as for applications where interfacing with various discrete components is required.

FIGURE 1–GATE COMPARISONS



MODIFIED DIODE-TRANSISTOR LOGIC

HIGH THRESHOLD LOGIC WITH PASSIVE PULLUP

FIGURE 2–TRANSFER CURVES

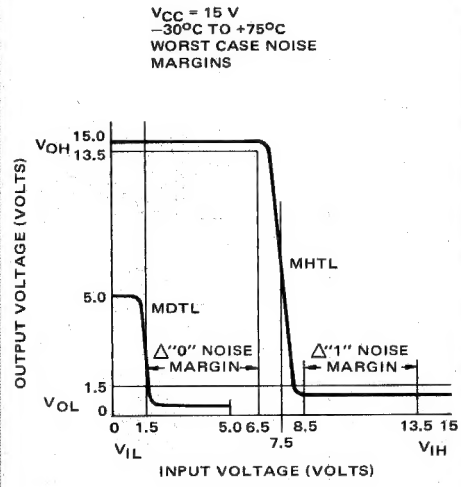
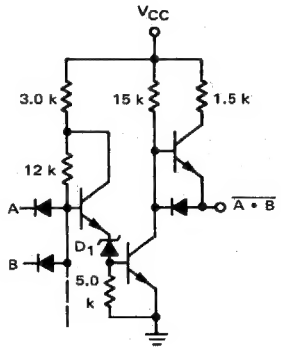
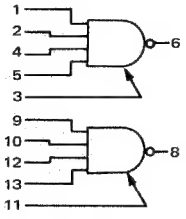


FIGURE 3–MHTL GATE WITH ACTIVE PULLUP



The logic diagrams shown describe the circuits of the MHTL line and permit quick selection of circuits required to implement a particular logic system. Pertinent information, such as logic equations and truth tables is provided to show line compatability. Package pin numbers and loading factors for each device are specified with each logic diagram. The numbers at the ends of the terminals are package pin numbers.

MC660P
EXPANDABLE DUAL 4-INPUT GATE
(with active output pullup)

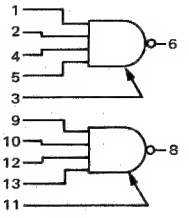


Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Inputs High - 88 mW
Inputs Low - 26 mW

MC661P
EXPANDABLE DUAL 4-INPUT GATE
(with passive output pullup)

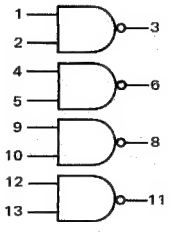


Positive Logic $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High - 88 mW
Inputs Low - 26 mW

MC668P
QUAD 2-INPUT GATE
(with passive output pullup)

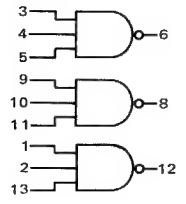


Positive Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High - 176 mW
Inputs Low - 52 mW

MC670P
TRIPLE 3-INPUT GATE
(with passive output pullup)

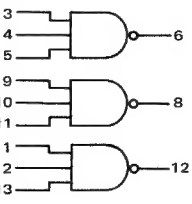


Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High - 132 mW
Inputs Low - 39 mW

MC671P
TRIPLE 3-INPUT GATE
(with active output pullup)

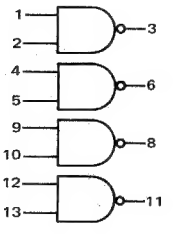


Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Inputs High - 132 mW
Inputs Low - 39 mW

MC672P
QUAD 2-INPUT GATE
(with active output pullup)



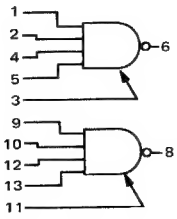
Positive Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Inputs High - 176 mW
Inputs Low - 52 mW

LOGIC DIAGRAMS (continued)

MC662P
EXPANDABLE
DUAL 4-INPUT LINE DRIVER
(with active output pullup)

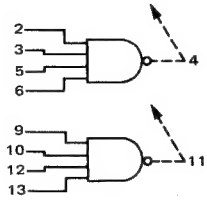


Positive Logic = $\overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

Input Loading Factor = 1
Output Loading Factor = 30

Propagation Delay Time = 140 ns typ
Typical Total Power Dissipation
Inputs High - 180 mW
Inputs Low - 26 mW

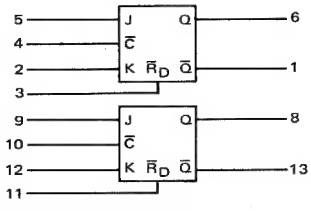
MC669P
DUAL 4-INPUT EXPANDERS



Positive Logic: $4 = \overline{2 \cdot 3 \cdot 5 \cdot 6}$

Input Loading Factor = 1

MC663P
DUAL J-K FLIP-FLOP



Input Loading Factor:
$\overline{R}_D$ Input = 2
$\overline{C}$ Input = 1.5
Other Inputs = 1
Output Loading Factor = 9

Total Power Dissipation = 200 mW typ
Toggle Frequency = 3.0 MHz typ

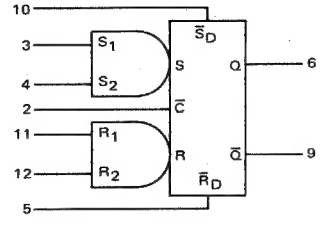
TRUTH TABLE

t_n		t_{n+1}	
J	K	Q	$\overline{Q}$
0	0	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
1	1	$\overline{Q}_n$	Q_n

Direct input ($\overline{R}_D$) must be high.
0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

NOTE: A low state "0" at the direct reset $\overline{R}_D$ causes a low state "0" at the Q output and the complement at the $\overline{Q}$ output.

MC664P
MASTER-SLAVE R-S FLIP-FLOP



Input Loading Factor:
$\overline{C}$ Input = 3
Other Inputs = 1
Output Loading Factor = 8

Total Power Dissipation = 160 mW typ
Toggle Frequency = 3.0 MHz typ

DIRECT INPUT OPERATION

$\overline{R}_D$	$\overline{S}_D$	Q	$\overline{Q}$
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

CLOCKED OPERATION*

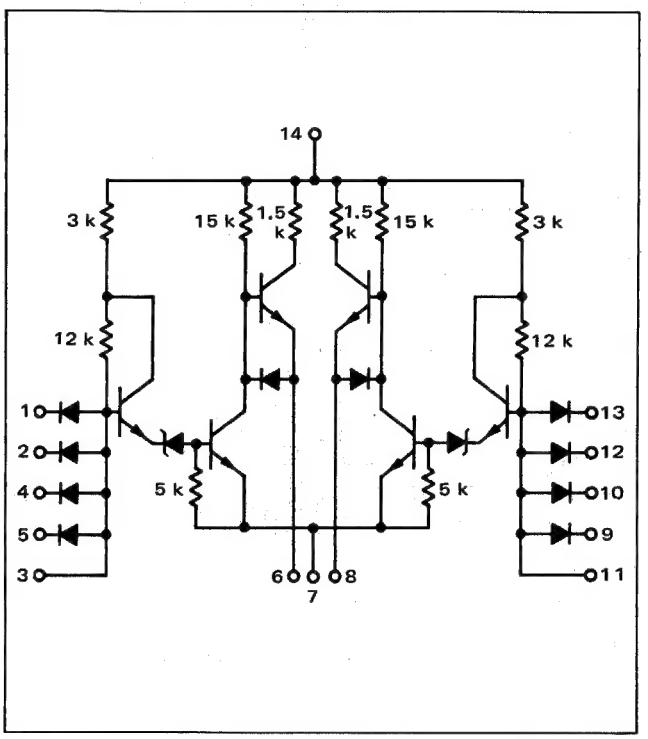
t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

* Direct inputs ($\overline{R}_D$, $\overline{S}_D$) must be high.

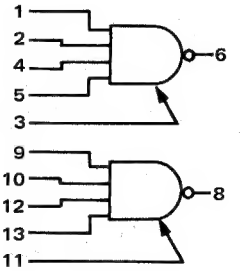
0 = low state
1 = high state
NC = No change
NA = Not allowed
X = state of input does not affect state of the circuit
U = indeterminate state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

EXPANDABLE DUAL 4-INPUT GATE

MC660P



This device consists of two expandable 4-input NAND gates with active output pullup.

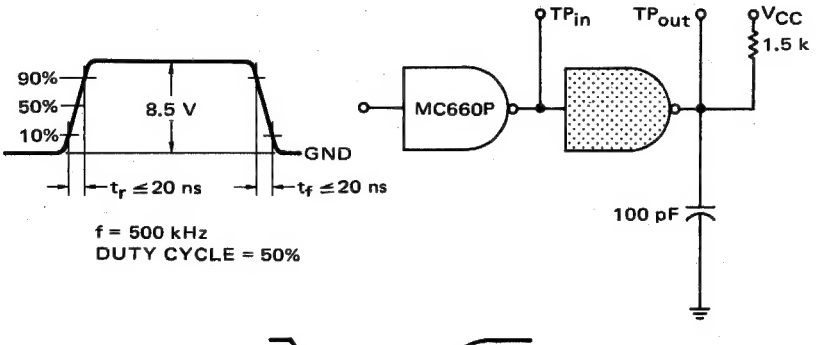


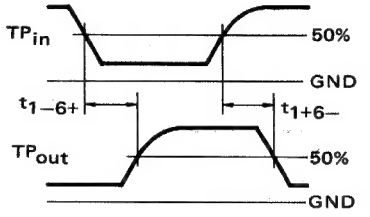
Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Input High = 88 mW
Inputs Low = 26 mW

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





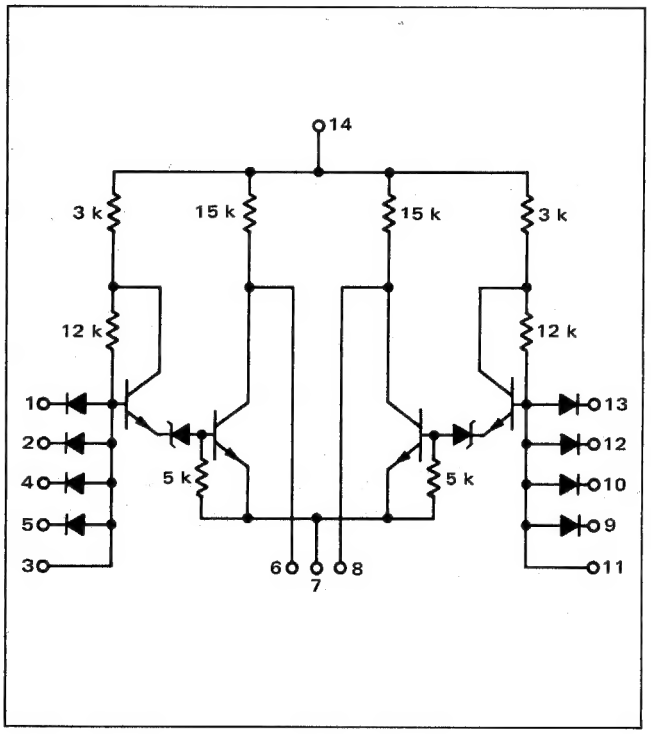
ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gate is tested in the same manner.

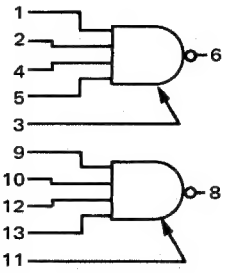
Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL} (mA)	I_{OH} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_X (Volts)	V_{CEX} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	Gnd
										TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
										12.0	-0.03	6.50	8.50	1.5	16.0	7.20	16.0	15.0	14.0	16.0	
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	1, 2, 4, 5	-	-	-	-	-	14	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-		-	6	1	-	-	-	-	-	2, 4, 5	14	-	
			-	-		-		-		-		2	-	-	-	-	-	1, 4, 5		-	
			-	-		-		-		-		4	-	-	-	-	-	1, 2, 5		-	
			-	-		-		-		-		5	-	-	-	-	-	1, 2, 4		-	
			-	-		-		-		-		-	-	-	-	3	-	-		-	
Short-Circuit Current	I_{SC}	6	-	-	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 6, 7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	-	14	-	2, 3, 4, 5, 7
		2	-	-	-		-			-	-	-	-	-	2	-	-	-		-	1, 3, 4, 5, 7
		4	-	-	-		-			-	-	-	-	-	4	-	-	-		-	1, 2, 3, 5, 7
		5	-	-	-		-			-	-	-	-	-	5	-	-	-		-	1, 2, 3, 4, 7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	-	6, 14	-	-	-	1, 7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2, 4, 5	-	-	-	-	14	7
		2	-	-	-		-			-	-	-	-	2	1, 4, 5	-	-	-	-		
		4	-	-	-		-			-	-	-	-	4	1, 2, 5	-	-	-	-		
		5	-	-	-		-			-	-	-	-	5	1, 2, 4	-	-	-	-		
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	3.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13
	I_{CCH}	14	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out										
	t_{1-6+}	6	-	-	-	200	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7
	t_{1+6-}	6	-	-	-	100	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

MC661P



This device consists of two expandable 4-input NAND gates with passive output pullup.

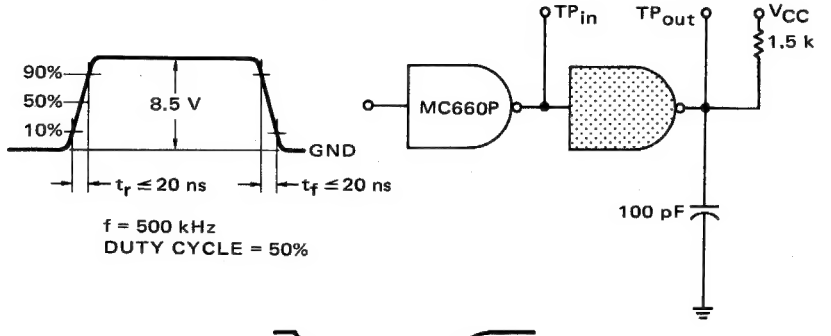


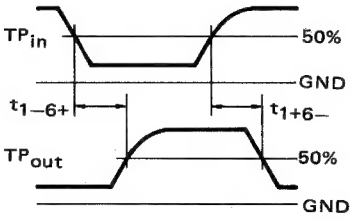
Positive Logic $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Input High = 88 mW
Inputs Low = 26 mW

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

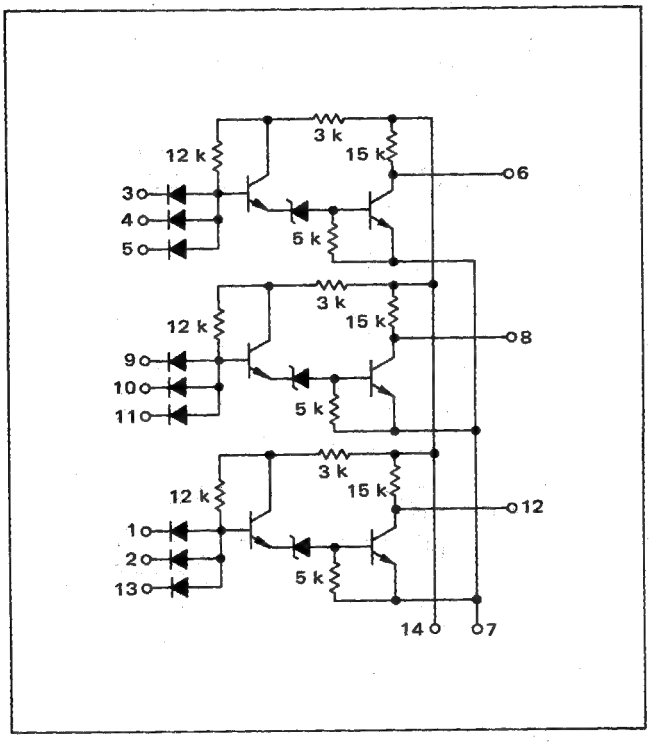
Test procedures are shown for one gate only.
The other gate is tested in the same manner.

Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_X	Volts V_{CEX}	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Gnd
										12.0	-0.03	6.50	8.50	1.5	16.0	7.20	16.0	15.0	14.0	16.0	
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
										I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_X	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	1, 2, 4, 5	-	-	-	-	-	14	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-		-	6	1	-	-	-	-	-	2, 4, 5	14	-	
			-	-		-		-		-		2	-	-	-	-	-	1, 4, 5		-	
			-	-		-		-		-		4	-	-	-	-	-	1, 2, 5		-	
			-	-		-		-		-		5	-	-	-	-	-	1, 2, 4		-	
			-	-		-		-		-		-	-	-	-	3	-	-		-	
Short-Circuit Current	I_{SC}	6	-	-	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 6, 7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	-	14	-	2, 3, 4, 5, 7
		2	-	-	-		-			-	-	-	-	-	2	-	-	-		-	1, 3, 4, 5, 7
		4	-	-	-		-			-	-	-	-	-	4	-	-	-		-	1, 2, 3, 5, 7
		5	-	-	-		-			-	-	-	-	-	5	-	-	-		-	1, 2, 3, 4, 7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	-	6, 14	-	-	-	1, 7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2, 4, 5	-	-	-	-	14	7
		2	-	-	-		-			-	-	-	-	2	1, 4, 5	-	-	-	-		
		4	-	-	-		-			-	-	-	-	4	1, 2, 5	-	-	-	-		
		5	-	-	-		-			-	-	-	-	5	1, 2, 4	-	-	-	-		
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	3.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13
	I_{CCH}	14	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out										
	t_{1-6+}	6	-	-	-	250	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7
	t_{1+6-}	6	-	-	-	100	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7

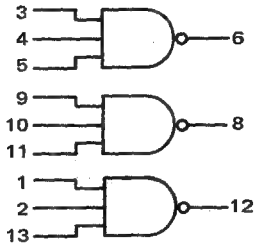
Pins not listed are left open.

TRIPLE 3-INPUT GATE

MC670P



This device consists of three 3-input NAND gates with passive output pull-up.

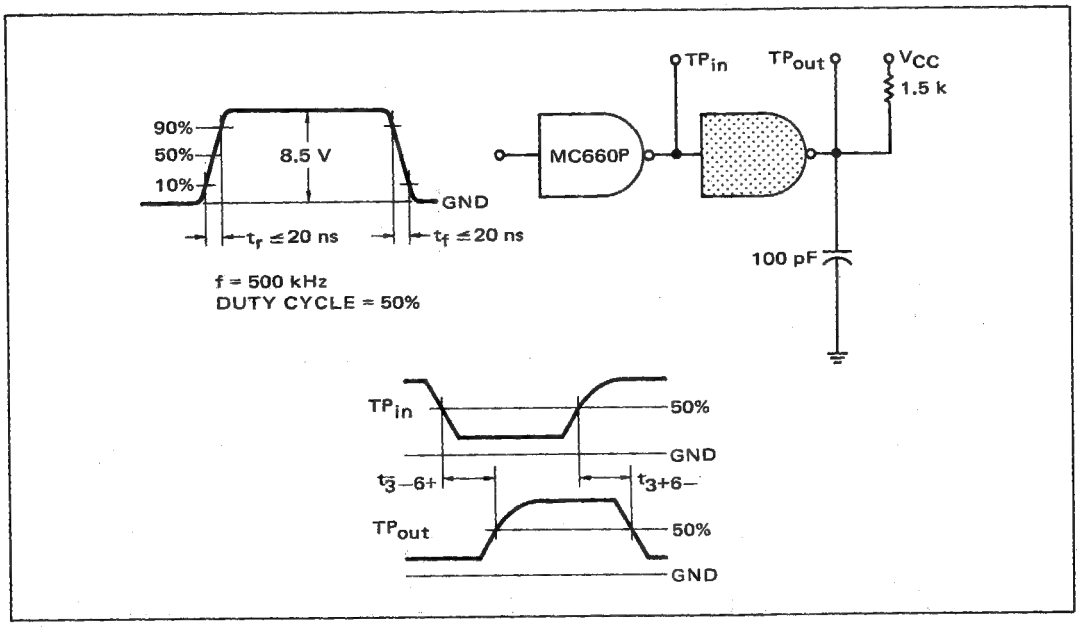


Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Input High = 132 mW
Inputs Low = 39 mW

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



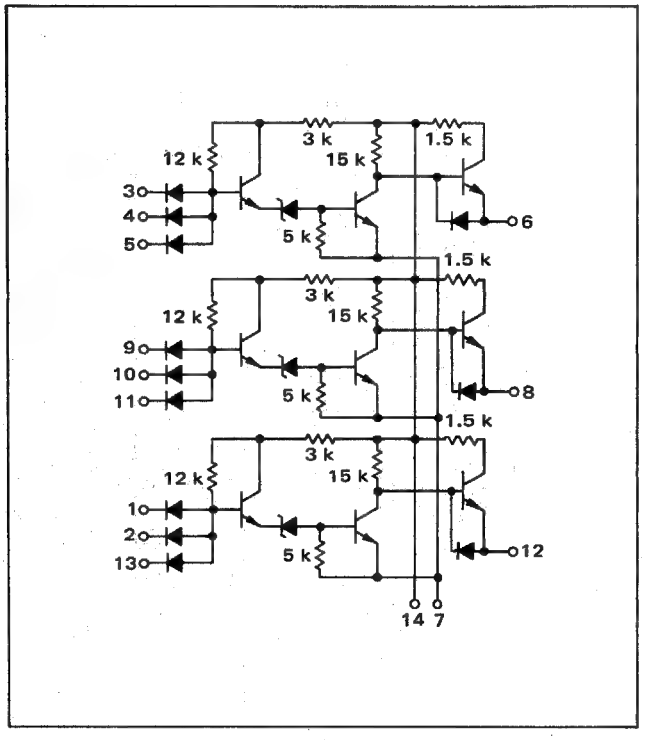
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate.
The other gates are tested in the same manner.

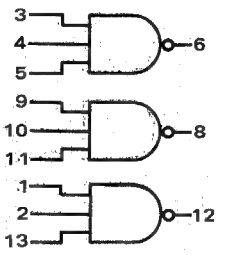
Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CEX}	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Gnd
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	3, 4, 5	-	-	-	-	14	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-	↓	-	6	3	-	-	-	-	4, 5	14	-	↓
		↓	-	-	↓	-	↓	-		-	↓	4	-	-	-	-	3, 5	↓	-	
			-	-		-		-		-		5	-	-	-	-	3, 4		-	
Short-Circuit Current	I_{SC}	6	-	-	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	14	3, 6, 7
Reverse Current	I_R	3	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	3	-	-	14	-	4, 5, 7
		4	-	-	-	↓	-	↓	↓	-	-	-	-	-	4	-	-	↓	-	3, 5, 7
		5	-	-	-		-			-	-	-	-	-	5	-	-		-	3, 4, 7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	6, 14	-	-	-	3, 7
Forward Current	I_F	3	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	3	4, 5	-	-	-	14	7
		4	-	-	-	↓	-	↓	↓	-	-	-	-	4	3, 5	-	-	-	↓	↓
		5	-	-	-		-			-	-	-	-	5	3, 4	-	-	-		
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	4.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1, 2, 3, 4, 5, 7, 9, 10, 11, 13
	I_{CCH}	14	-	-	-	15	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out									
	t_{3-6+}	6	-	-	-	250	-	-	ns	3	6	-	-	-	-	-	14	-	-	7
	t_{3+6-}	6	-	-	-	100	-	-	ns	3	6	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

MC671P



This device consists of three 3-input NAND gates with active output pull-up.

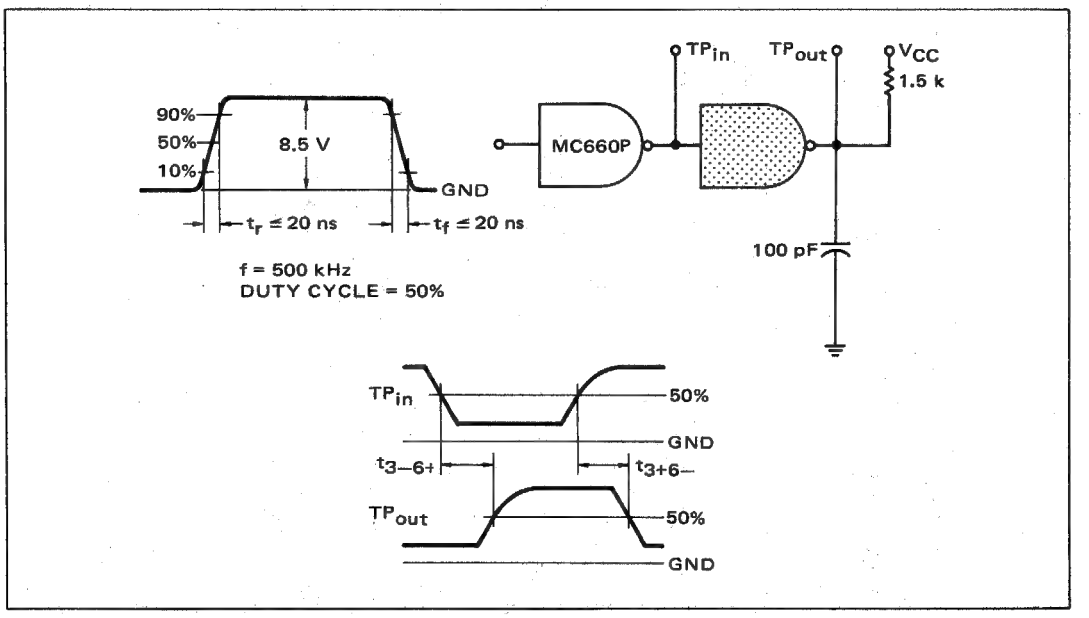


Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Input High = 132 mW
Inputs Low = 39 mW

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



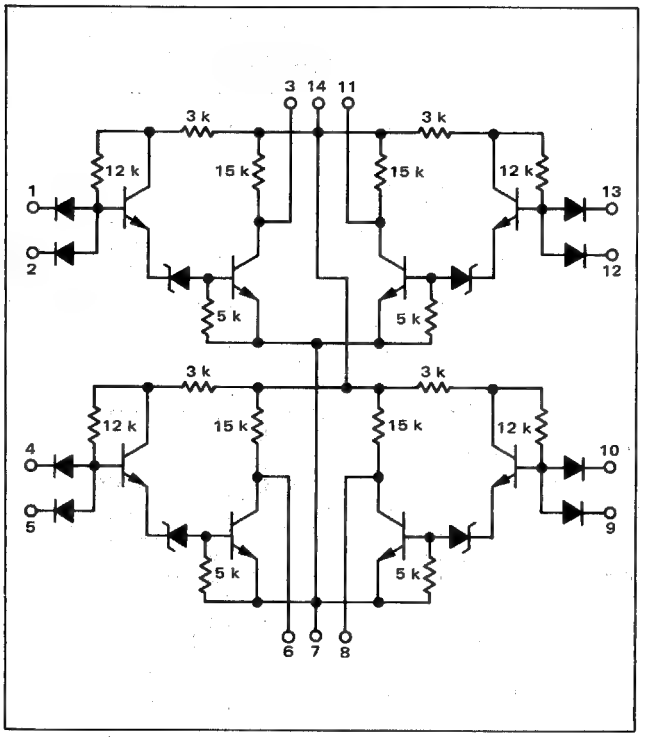
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate.
The other gates are tested in the same manner.

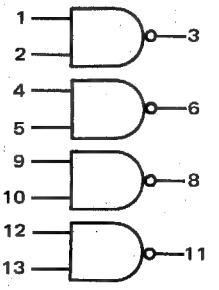
			TEST LIMITS							TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:									
			−30°C		+25°C		+75°C			TEST CURRENT/VOLTAGE VALUES (All Temperatures)									
										mA		Volts							
Characteristic	Symbol	Pin Under Test	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	3,4,5	-	-	-	-	14	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-	Vdc	-	6	3	-	-	-	-	4,5	14	-	↓
		↓	-	-	↓	-	↓	-	↓	-	↓	4	-	-	-	-	3,5	↓	-	
			-	-		-		-		-		5	-	-	-	-	3,4		-	
Short-Circuit Current	I_{SC}	6	-	-	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	-	-	-	14	3,6,7
Reverse Current	I_R	3	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	3	-	-	14	-	4,5,7
		4	-	-	-	↓	-	↓	↓	-	-	-	-	-	4	-	-	↓	-	3,5,7
		5	-	-	-		-			-	-	-	-	-	5	-	-		-	3,4,7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	6,14	-	-	-	3,7
Forward Current	I_F	3	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	3	4,5	-	-	-	14	7
		4	-	-	-	↓	-	↓	↓	-	-	-	-	4	3,5	-	-	-	↓	↓
		5	-	-	-		-			-	-	-	-	5	3,4	-	-	-		
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	4.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1,2,3,4,5,7, 9,10,11,13
	I_{CCH}	14	-	-	-	15	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out									
	t_{3-6+}	6	-	-	-	200	-	-	ns	3	6	-	-	-	-	-	14	-	-	7
	t_{3+6-}	6	-	-	-	100	-	-	ns	3	6	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

MC668P



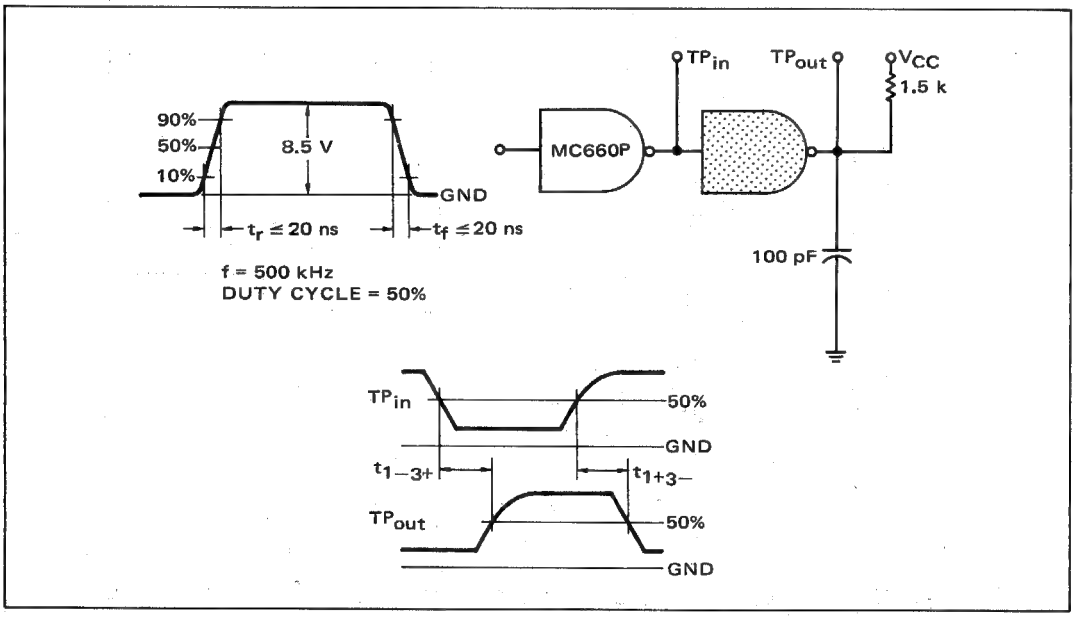
This device consists of four 2-input NAND gates with passive output pull-up.



Positive Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Input High = 176 mW
Inputs Low = 52 mW

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



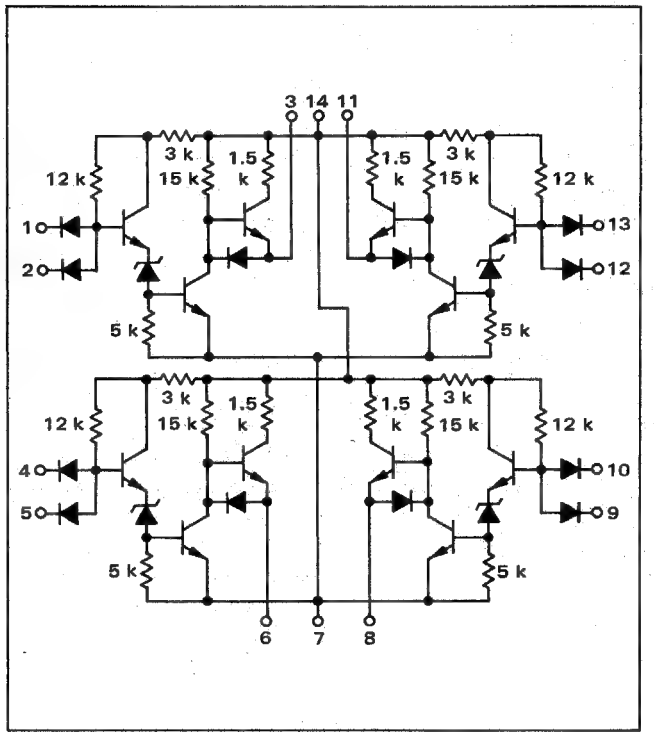
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate.
The other gates are tested in the same manner.

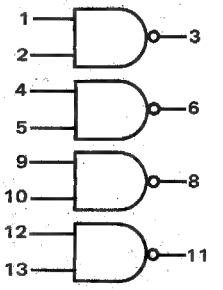
										TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
										mA		Volts								
										I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
			TEST LIMITS							TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
			−30°C		+25°C		+75°C													
Characteristic	Symbol	Pin Under Test	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	3	-	1.5	-	1.5	-	1.5	Vdc	3	-	-	1,2	-	-	-	-	14	-	7
	V_{OH}	3	-	-	12.5	-	12.5	-	↓	-	3	1	-	-	-	-	2	14	-	↓
		3	-	-	12.5	-	12.5	-		-	3	2	-	-	-	-	1	14	-	
Short-Circuit Current	I_{SC}	3	-	-	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	14	1,3,7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	14	-	2,7
		2	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	2	-	-	14	-	1,7
Output Leakage Current	I_{CEX}	3	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	3,14	-	-	-	1,7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2	-	-	-	14	7
		2	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	2	1	-	-	-	14	7
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	6.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1,2,4,5,7, 9,10,12,13
	I_{CCH}	14	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out									
	t_{1-3+}	3	-	-	-	250	-	-	ns	1	3	-	-	-	-	-	14	-	-	7
	t_{1+3-}	3	-	-	-	100	-	-	ns	1	3	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

MC672P



This device consists of four 2-input NAND gates with active output pull-up.



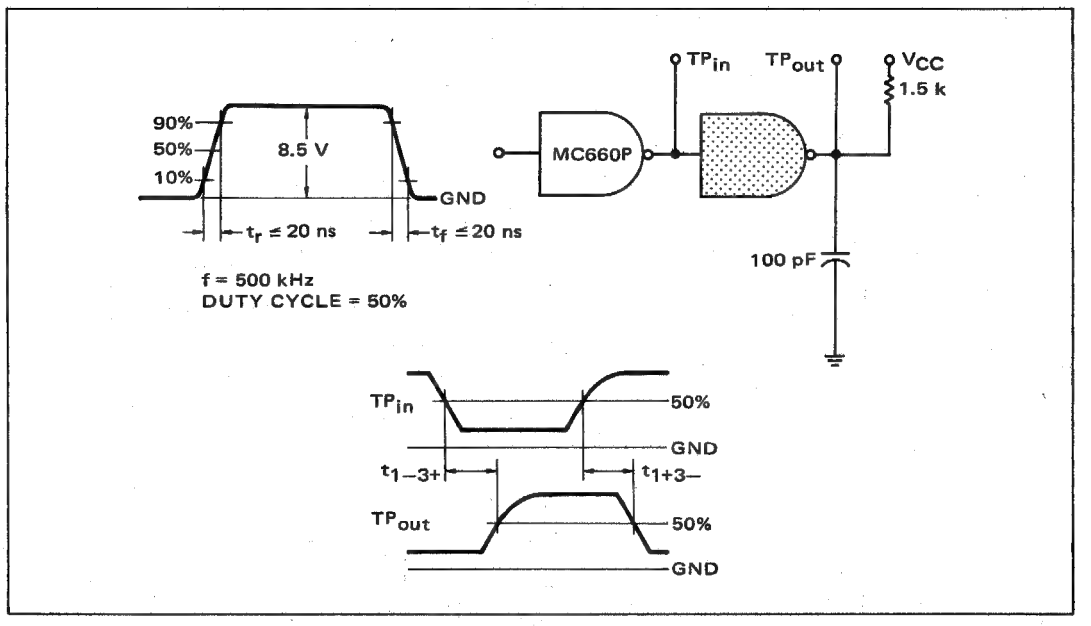
Positive Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation

Input High = 176 mW
Inputs Low = 52 mW

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



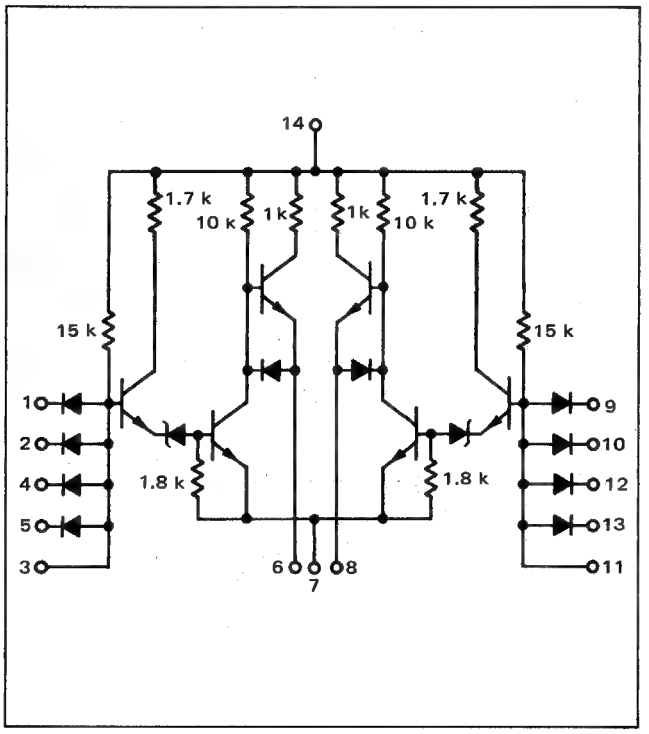
ELECTRICAL CHARACTERISTICS

Test procedures shown are for one gate only.
The other gates are tested in the same manner.

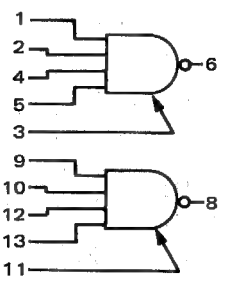
			TEST LIMITS							TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
										mA		Volts								
										I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
			−30°C		+25°C		+75°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
Characteristic	Symbol	Pin Under Test	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	3	-	1.5	-	1.5	-	1.5	Vdc	3	-	-	1, 2	-	-	-	-	14	-	7
	V_{OH}	3	-	-	12.5	-	12.5	-	Vdc	-	3	1	-	-	-	-	2	14	-	7
		3	-	-	12.5	-	12.5	-	Vdc	-	3	2	-	-	-	-	1	14	-	7
Short-Circuit Current	I_{SC}	3	-	-	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	-	-	-	14	1, 3, 7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	14	-	2, 7
		2	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	2	-	-	14	-	1, 7
Output Leakage Current	I_{CEX}	3	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	3, 14	-	-	-	1, 7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2	-	-	-	14	7
		2	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	2	1	-	-	-	14	7
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	6.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13
	I_{CCH}	14	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out									
	t_{1-3+}	3	-	-	-	200	-	-	ns	1	3	-	-	-	-	-	14	-	-	7
	t_{1+3-}	3	-	-	-	100	-	-	ns	1	3	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

MC662P



This device consists of two expandable 4-input NAND line drivers with active output pullup. This device allows fan-out to 30 MHTL gates and drives large capacitive loads.

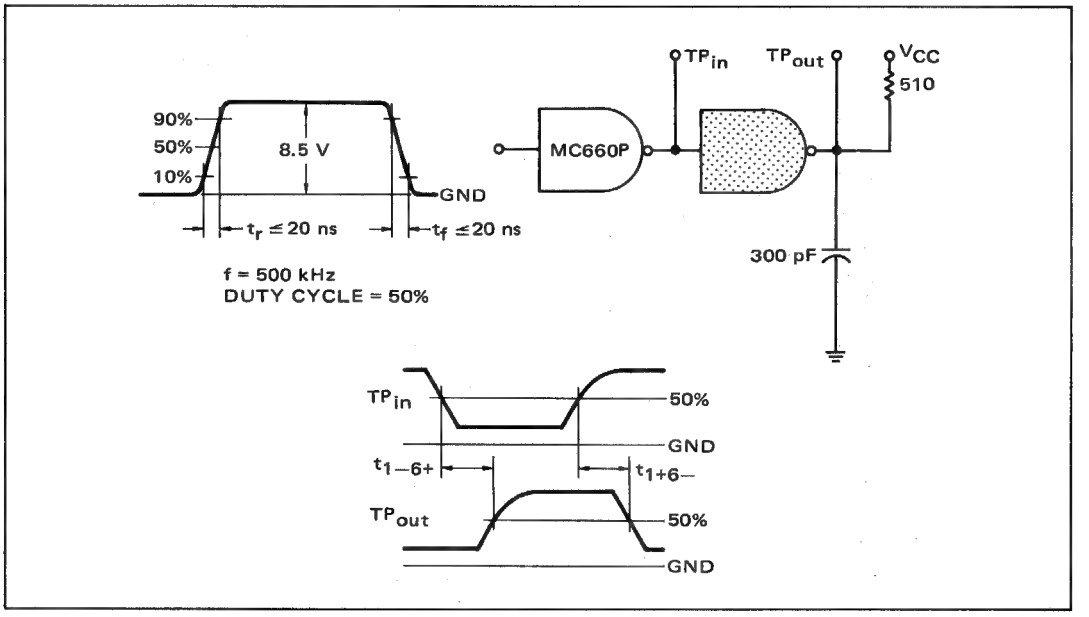


Positive Logic = $\overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

Input Loading Factor = 1
Output Loading Factor = 30

Propagation Delay Time = 140 ns typ
Typical Total Power Dissipation
Input High = 180 mW
Inputs Low = 26 mW

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

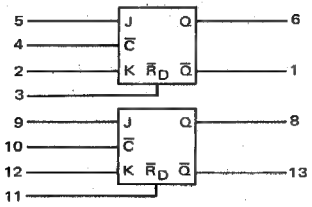
Test procedures are shown for one driver only.
The other driver is tested in the same manner.

Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_X	Volts V_{CEX}	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Gnd
										36.0	-0.09	6.50	8.50	1.5	16.0	7.20	16.0	15.0	14.0	16.0	
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
										I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_X	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	1, 2, 4, 5	-	-	-	-	-	14	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-		-	6	1	-	-	-	-	-	2, 4, 5	14	-	
			-	-		-		-		-		2	-	-	-	-	-	1, 4, 5		-	
			-	-		-		-		-		4	-	-	-	-	-	1, 2, 5		-	
			-	-		-		-		-		5	-	-	-	-	-	1, 2, 4		-	
			-	-		-		-		-		-	-	-	-	3	-	-		-	
Short-Circut Current	I_{SC}	6	-	-	-10.0	-25.0	-10.0	-25.0	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 6, 7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	-	14	-	2, 3, 4, 5, 7
		2	-	-	-		-			-	-	-	-	-	2	-	-	-		-	1, 3, 4, 5, 7
		4	-	-	-		-			-	-	-	-	-	4	-	-	-		-	1, 2, 4, 5, 7
		5	-	-	-		-			-	-	-	-	-	5	-	-	-		-	1, 2, 3, 4, 7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	-	6, 14	-	-	-	1, 7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2, 4, 5	-	-	-	-	14	7
		2	-	-	-		-			-	-	-	-	2	1, 4, 5	-	-	-	-		
		4	-	-	-		-			-	-	-	-	4	1, 2, 5	-	-	-	-		
		5	-	-	-		-			-	-	-	-	5	1, 2, 4	-	-	-	-		
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	4.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13
	I_{CCH}	14	-	-	-	17	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out										
	t_{1-6+}	6	-	-	-	250	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7
	t_{1+6-}	6	-	-	-	100	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

MC663P

Two J-K flip-flops in a single package. Each flip-flop has a direct reset input in addition to the clocked inputs.



TRUTH TABLE

t_n		t_{n+1}	
J	K	Q	$\bar{Q}$
0	0	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
1	1	$\bar{Q}_n$	Q_n

Input Loading Factor:
$\bar{R}_D$ Input = 2
$\bar{C}$ Input = 1.5
Other Inputs = 1

Output Loading Factor = 9

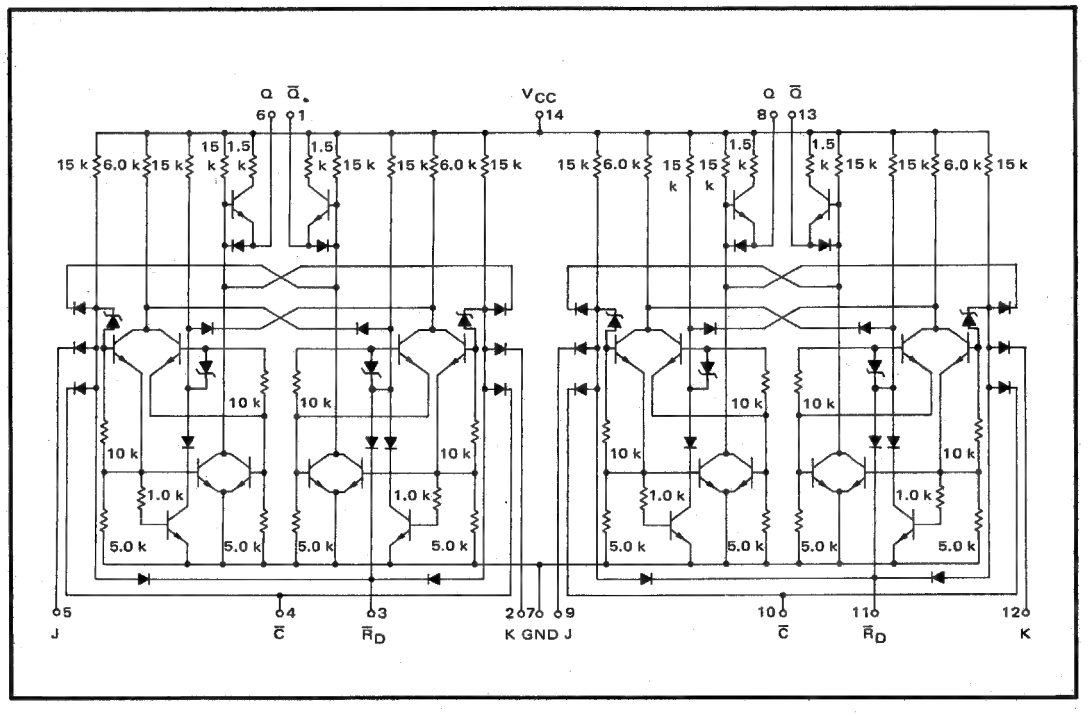
Loading factors are valid from −30°C to +75°C with V_{CC} = 15 ± 1 Vdc

f_{Tog} = 3.0 MHz typ

Total Power Dissipation = 200 mW typ

Direct input ($\bar{R}_D$) must be high.
0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

NOTE: A low state "0" at the direct reset $\bar{R}_D$ causes a low state "0" at the Q output and the complement at the $\bar{Q}$ output.

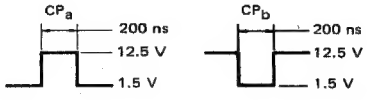


ELECTRICAL CHARACTERISTICS

Unless otherwise noted, tests are shown for only one flip-flop. The other flip-flop is tested in the same manner.

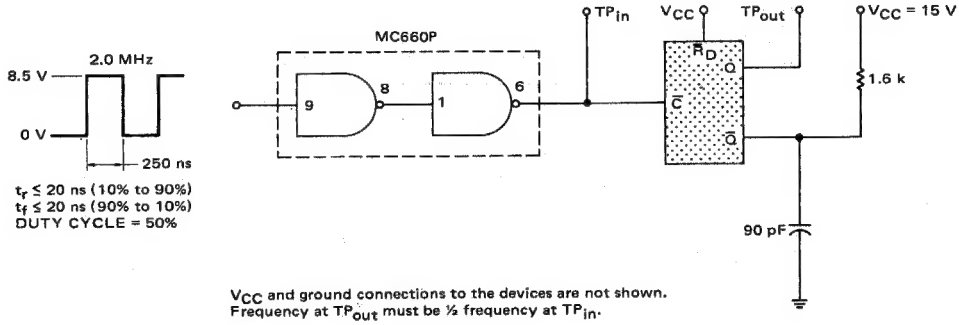
Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL} (mA)	I_{OH} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	CP_a	CP_b	Ground
										10.8	-0.027	6.50	8.50	1.5	16.0	14.0	16.0			
Output Voltage	V_{OL}	1	-	1.5	-	1.5	-	1.5	Vdc	1	-	2	3,5	-	-	14	-	4	-	7
		6	-	1.5	-	1.5	-	1.5		6	-	5	2,3	-	-	14	-	4	-	7
	V_{OH}	1	-	-	12.5	-	12.5	-		-	1	2,3	5	-	-	14	-	4	-	7
		1	-	-	12.5	-	12.5	-		-	1	5	2,3	-	-	14	-	4	-	7
		6	-	-	12.5	-	12.5	-		-	6	2	3,5	-	-	14	-	4	-	7
Short-Circuit Current	I_{SC}	1	-	-	-6.5	-15	-6.5	-15	mAdc	-	-	3,4	-	-	-	-	14	-	-	1,7
Reverse Current	I_R	2	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	2	14	-	-	-	3,4,5,7
	$3I_R$	3	-	-	-	6.0	-	6.0		-	-	-	-	-	3	2,4,5,14	-	-	-	7
	$2I_R$	4	-	-	-	4.0	-	4.0		-	-	-	-	-	4	14	-	-	-	2,3,5,7
	I_R	5	-	-	-	2.0	-	2.0		-	-	-	-	-	5	14	-	-	-	2,3,4,7
Forward Current	I_F	2	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	2	-	-	14	-	4	7
		3	-	-	-	-1.20	-	-1.20		-	-	-	-	3	-	-	14	-	-	2,4,5,7
		4	-	-	-	-1.20	-	-1.20		-	-	-	-	4	-	-	2,5,14	-	-	7
		5	-	-	-	-1.20	-	-1.20		-	-	-	-	5	-	-	14	-	4	7
Power Drain Current (Both Flip-Flops)	I_{CCL}	14	-	-	-	16.7	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	2,3,4,5,7,9,10,11,12
	I_{CCH}	14	-	-	-	16.7	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.



$t_r \leq 1.0\ \mu s$ (10% to 90%)
$t_f \leq 1.0\ \mu s$ (90% to 10%)

TOGGLE MODE TEST CIRCUIT

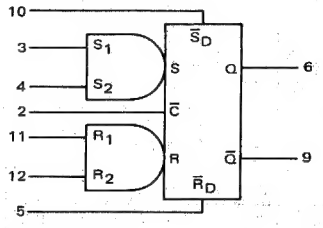


$t_r \leq 20$ ns (10% to 90%)
$t_f \leq 20$ ns (90% to 10%)
DUTY CYCLE = 50%

V_{CC} and ground connections to the devices are not shown.
Frequency at TP_{out} must be ½ frequency at TP_{in}.

MC664P

A dc coupled R-S flip-flop operating on the master-slave principle. Information is entered in the master section while the clock pulse is high and is transferred to the slave when the clock goes negative.



Input Loading Factor:
$\overline{C}$ Input = 3
Other Inputs = 1

Output Loading Factor = 8

Loading factors are valid from −30°C to +75°C with V_{CC} = 15 ± 1 Vdc

f_{Tog} = 3.0 MHz typ

Total Power Dissipation = 160 mW typ

DIRECT INPUT OPERATION

$\overline{R}_D$	$\overline{S}_D$	Q	$\overline{Q}$
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

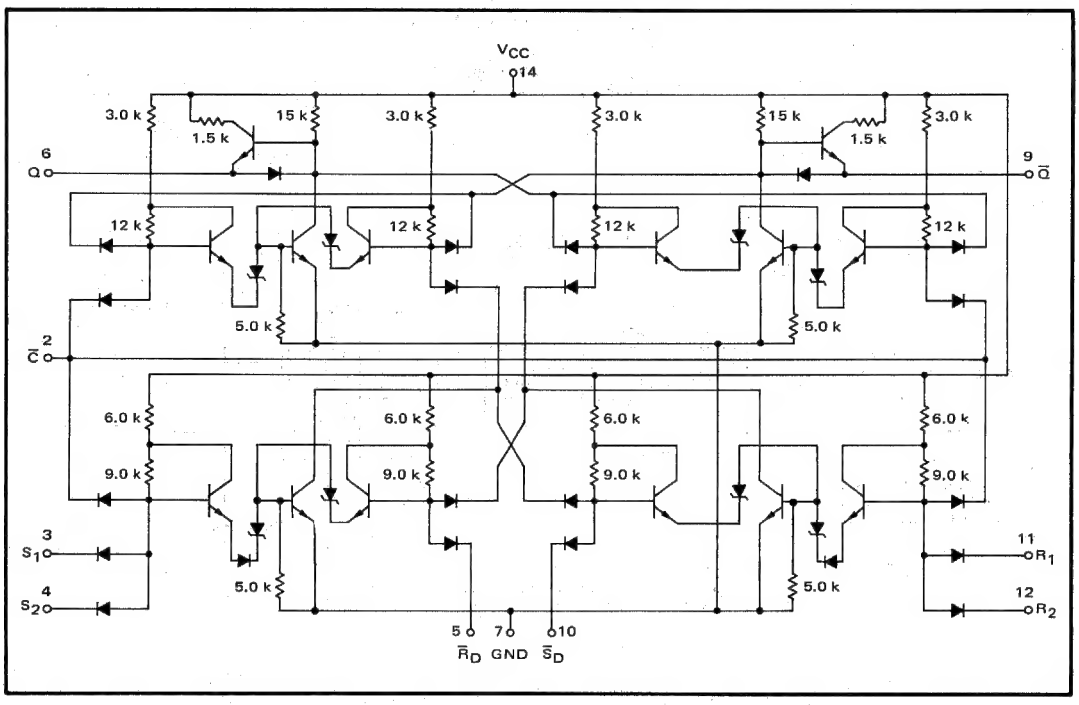
NC = No change
NA = Not allowed

CLOCKED OPERATION

t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

NOTES FOR CLOCKED-OPERATION TRUTH TABLE:

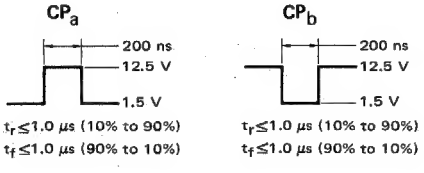
Direct inputs ($\overline{R}_D$, $\overline{S}_D$) must be high.
0 = low state
1 = high state
X = state of input does not affect state of the circuit
U = indeterminate state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n



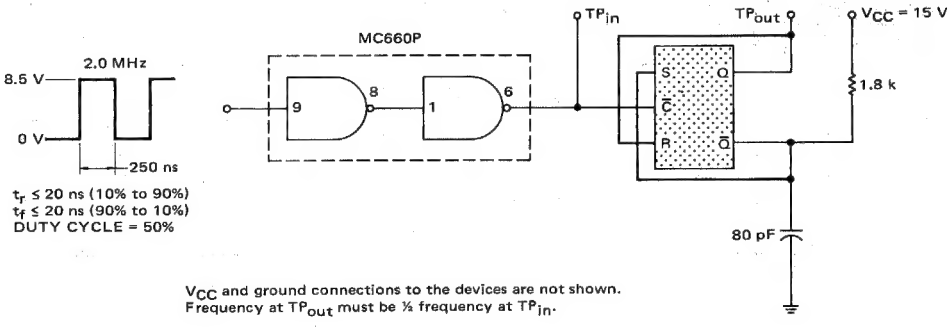
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL} (mA)	I_{OH} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	CP_a	CP_b	Ground
										9.6	-0.024	6.50	8.50	1.5	16.0	14.0	16.0			
Output Voltage	V_{OL}	6*	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	3, 4, 11, 12	-	-	14	-	-	5	7
		6	-	↓	-	↓	-	↓		6	-	4	3, 5, 11, 12	-	-	↓	-	2	-	7
		6	-		-		-			6	-	3	4, 5, 11, 12	-	-		-	2	-	7
		9‡	-		-		-			9	-	-	3, 4, 11, 12	-	-		-	-	10	7
		9	-		-		-			9	-	11	3, 4, 10, 12	-	-		-	2	-	7
		9	-		-		-			9	-	12	3, 4, 10, 11	-	-		-	2	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-		-	6	-	5	-	-	14	-	-	-	2, 3, 4, 7, 10, 11, 12
		9	-	-	12.5	-	12.5	-		-	9	-	10	-	-	14	-	-	-	2, 3, 4, 5, 7, 11, 12
Short-Circuit Current	I_{SC}	6	-	-	-6.5	-15	-6.5	-15	mAdc	-	-	2, 5	10	-	-	-	14	-	-	6, 7, 9
		9	-	-	-6.5	-15	-6.5	-15	mAdc	-	-	2, 10	5	-	-	-	14	-	-	6, 7, 9
Reverse Current	$4I_R$	2§	-	-	-	8.0	-	8.0	μAdc	-	-	-	5	-	2	14	-	-	-	3, 4, 7, 10, 11, 12
	$4I_R$	2†	-	-	-	8.0	-	8.0		-	-	-	10	-	2	14	-	-	-	3, 4, 5, 7, 11, 12
	I_R	3	-	-	-	2.0	-	2.0		-	-	-	-	-	3	14	-	-	-	2, 4, 7
		4	-	-	-	↓	-	↓		-	-	-	-	-	4	14	-	-	-	2, 3, 7
		5	-	-	-		-			-	-	-	2, 11, 12	-	5	14	-	-	-	7
		10	-	-	-		-			-	-	-	2, 3, 4	-	10	14	-	-	-	7
		11	-	-	-		-			-	-	-	-	-	11	14	-	-	-	2, 7, 12
		12	-	-	-		-			-	-	-	-	-	12	14	-	-	-	2, 7, 11
Forward Current	$3I_F$	2	-	-	-	-3.60	-	-3.60	mAdc	-	-	-	5	2	3, 4, 11, 12	-	14	-	-	7, 10
	$3I_F$	2	-	-	-	-3.60	-	-3.60		-	-	-	10	2	3, 4, 11, 12	-	14	-	-	5, 7
	I_F	3	-	-	-	-1.20	-	-1.20		-	-	-	-	3	2, 4	-	14	-	-	7
		4	-	-	-	↓	-	↓		-	-	-	-	4	2, 3	-	14	-	-	7
		5	-	-	-		-			-	-	-	-	5	-	-	14	-	-	2, 7, 10, 11, 12
		10	-	-	-		-			-	-	-	-	10	-	-	14	-	-	2, 3, 4, 5, 7
		11	-	-	-		-			-	-	-	-	11	2, 12	-	14	-	-	7
		12	-	-	-	↓	-	↓		-	-	-	-	12	2, 11	-	14	-	-	7
Power Drain Current	I_{CCL}	14	-	-	-	14.5	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	2, 3, 4, 5, 7, 10, 11, 12
	I_{CCH}	14	-	-	-	14.5	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.
*Apply momentary ground to pins 9 and 10 prior to clock pulse
‡Apply momentary ground to pins 5 and 6 prior to clock pulse
§Apply momentary ground to pin 9
†Apply momentary ground to pin 6

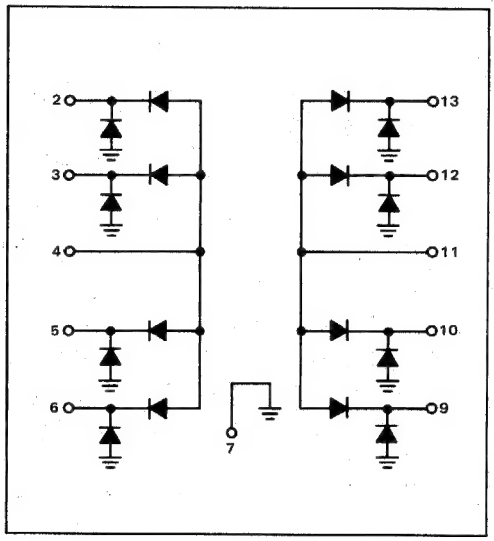


TOGGLE MODE TEST CIRCUIT

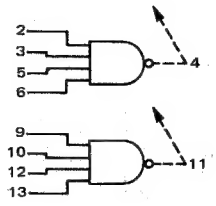


V_{CC} and ground connections to the devices are not shown.
Frequency at TP_{out} must be ½ frequency at TP_{in}.

MC669P



This device consists of two independent high voltage diode networks with characteristics matched to the input of the gate and buffer elements in the MHTL logic family. Its use increases the fan-in capability of other MHTL devices to a maximum of 20 while having negligible effect on their performance.



Positive Logic: $4 = \overline{2 \cdot 3 \cdot 5 \cdot 6}$

Input Loading Factor = 1

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in the same manner.

			TEST LIMITS							TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:		
			−30°C		+25°C		+75°C					
Characteristic	Symbol	Pin Under Test	Min	Max	Min	Max	Min	Max	Unit	I_F	V_R	Gnd
Forward Voltage	V_F	4	-	1.0	-	0.9	-	0.8	Vdc	4	-	2,7
			-		-		-				-	3,7
			-		-		-				-	5,7
			-		-		-				-	6,7
Reverse Current	I_R	2	-	2.0	-	2.0	-	2.0	μAdc	-	2	3,5,6,7
		3	-		-		-			-	3	2,5,6,7
		5	-		-		-			-	5	2,3,6,7
		6	-		-		-			-	6	2,3,5,7
	$2\,I_R$	4	-	-	-	4.0	-	-		-	4	7

TEST CURRENT/VOLTAGE VALUES (All Temperatures)	
mA	Volts
I_F	V_R
1.2	16.0

Pins not listed are left open